MULTICHANNEL DIGITAL SYNCHRONOUS INTEGRATOR

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ABSTRACT. *Multichannel synchronous integrator employed in the digital complex of acousto-optical analyzer is described. Functional scheme is presented and its detail operation in different modes is considered. Some possibilities of the integrator application in different multichannel systems are outlined. It is pointed out that the integrator has a wide application range in experiments from time resolution of a few ms to integration time of tens of seconds.*

Esepkina et al. (1990) have described the digital complex of the acousto-optical spectrum analyzer, which was developed in cooperation of SAO and St.Petersburg State Technical University collaborators.

An essential part of the above mentioned digital complex is a multichannel digital synchronous integrator (DSI). The DSI is intended for data reception and primary processing in the internal memory for a constant time of digitized pixels of CCD or any other multichannel devices, information storage, and its transfer into a computer. Since the employment of the DSI is possible in different multichannel systems of data acquisition such as acousto-optical or filter spectrum analyzers and other systems, the authors considered it expedient to describe the DSI operation in more detail.

A description of equipment with similar functions was presented earlier (Bowman, 1985; Gatenby, 1989; Wattenbach and Roser, 1985). Basic trend in the development of

digital complexes is to transfer the routine functions of data acquisition to hardware. To realize it, microprocessors and microschemes of high integration level are used. From the very beginning of DSI designing, the authors tried to optimize function of data acquisition, analysis, registration, and visualization of results between software and hardware, to create a device for different spectral researches based on widespread microschemes and notexpensive computers.

The common functional scheme of the system, assembling multichannel digital integrator, is shown in Fig.1. Instead of acousto-optical analyzer in this scheme it is possible to include any other multichannel device with the sequential channel sampling. This system operation and input of digitized information into DSI are under control of the system controller.

The DSI has been designed and produced in CAMAC standard. It gives an opportunity to use the DSI irrespective of a computer type.

As it is shown in Fig.1, signals of module selection CIN, frequency modulation F from the system controller, ADC code and termination of À/D conversion END enter the DSI through the front panel.
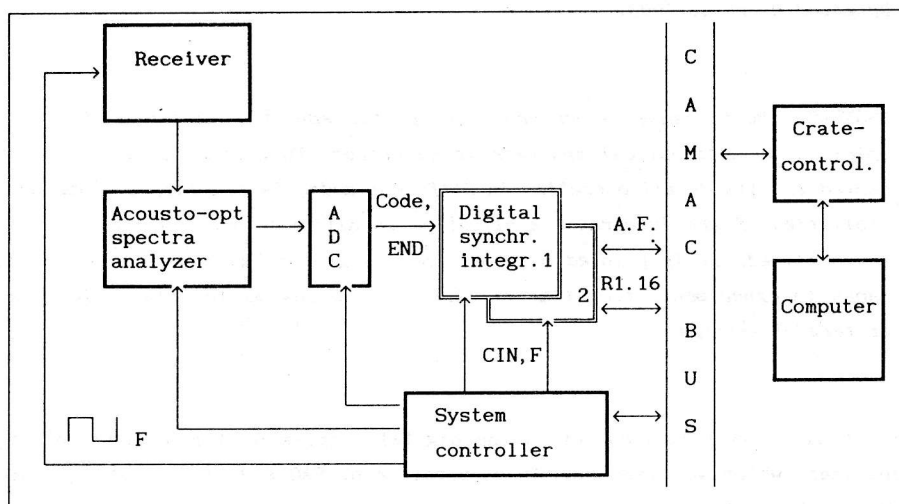

Fig.1. *Functional scheme of the spectral complex.*

Readout of the integrated information to the computer memory for the following processing is provided by CAMAC bus under the program control. Time relationship of the incoming external signals is shown in Fig.3.

In order to avoid the data loss because of time coincidence of input and output processes, it is necessary to employ two identical DSIs. One integrator takes ADC codes and the other reads out the integration result to the computer simultaneously.

As it is shown in Fig.2 there are the following main units in DSI:
- buffer storage of 4096 × 16 bits (RAM)
- arithmetic and logic unit (ALU)

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- instruction register
- address counter
- output register
- control scheme
- input and output logic schemes.

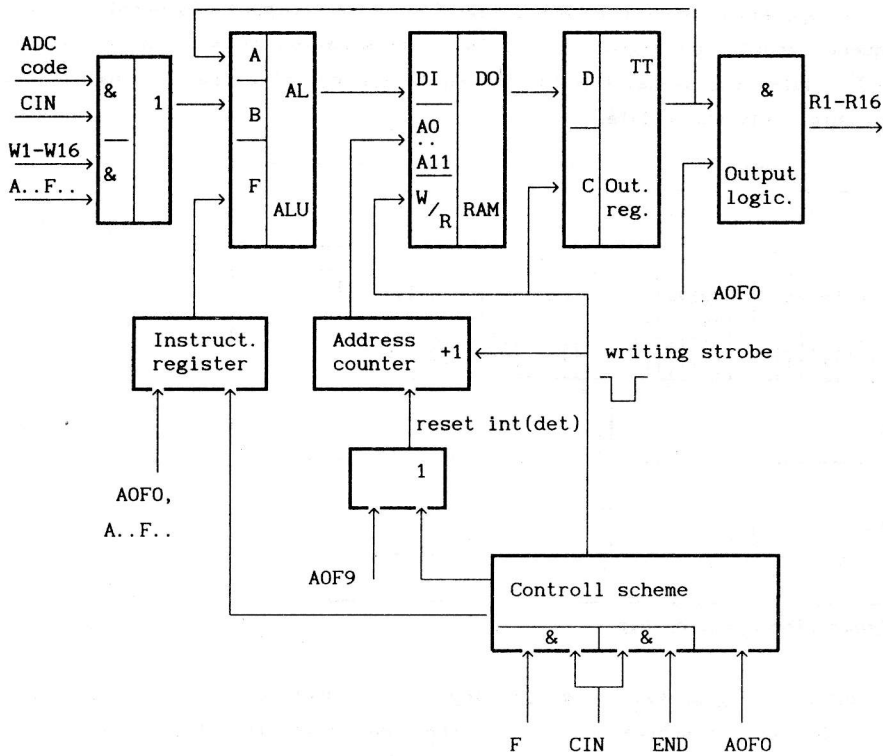Links between the DSI main units are shown in Fig.2 also.

Fig.2. *Functional scheme of multichannel synchronous integrator.*

ALU performs the following functions:

1. Summation of digitized samples of the spectral channels with the ones which are loaded into the buffer store.

2. Subtraction of digitized samples of the spectral channel from the current result in the buffer store.

3. Transmission of data from a computer to the buffer store for DSI test.

4. Setting up of logical zero for the buffer store clearing.

All ALU functions are determined by instruction register contents. An address counter defines sequential access to the buffer store cells. Synchronization of all DSI units operations is carried out by the control scheme, which sets up the order of operation of instruction register, ALU, address counter, buffer store and output

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register.

DSI may be used in the following modes:

1. Data reception and primary data processing;

2. Data readout and buffer store clearing;

3. Testing of the DSI units.

In its turn the first mode may be realized in two ways - synchronous integration and detection.

Consider DSI operation in synchronous integration mode. Signal CIN permits entering of frequency modulation signal F, and END - termination of A/D conversion. To different DSI modules the signal CIN is applied in the opposite phases, that is why ADC code can enter only one module.
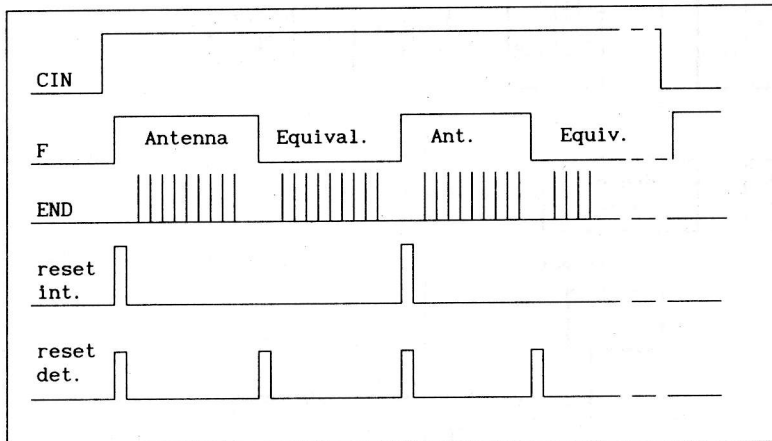

Fig.3. *Signal-time relationship.*

As it is shown in Fig.3, switching F to logical 1 causes the signal "reset(int)" generation in the control scheme and sets in the instruction register a code, which corresponds to "A+B" ALU function. Here "A" is the current addressed memory contents and "B" is ADC code. Signal "reset" applied to address counter initiates it. Every signal END causes the writing strobe generation. Its front pulse produces in the output register latching of data, which are held in the currently addressed buffer store cell. During the logical 0 state of the strobe, ALU sums ADC code and output register contents, transfers the result into the same memory address. The rear front of the strobe increments address counter. The next signal F switching to logical 1 resets address counter again and the following series of ADC codes will be summed with the current values of the buffer store in the way considered above. Integration will last as long as the signal CIN disables one DSI module and enables another. As a result the DSI buffer store will contain two data files corresponding to "Antenna" and "Equivalent" phases. If a_{ki} is assigned as digitized k-th frequency channel sample in i-th modulation period and an integration time duration is N of modulation periods,

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then the final result may be expressed as follows:

$$A = \left\{ \sum_{i=0}^{N-1} a_{ki} \;\middle|\; k=1,2,\ldots K \right\},$$

$$E = \left\{ \sum_{i=0}^{N-1} e_{ki} \;\middle|\; k=1,2,\ldots K \right\},$$

where A and E are the files of integrated samples of spectral channels in "Antenna" and "Equivalent" phases, respectively, K is CCD pixels or the filter channels number. The file A occupies the buffer store cells from 0 to $K-1$, and file E - from K to $2K-1$ above. As a result it takes $2K$ storage cells for two data files.

Before the data readout a computer needs to define in what DSI module information is. CIN signal absence indicates a module for readout. CAMAC command AOF9 generates signal "reset", which causes initiation of the address counter. Afterwards with every subsequent CAMAC command AOF0, a computer outputs an integrated information of one channel of the analyzer. The way in which DIS outputs an information is similar to that in which the data are loaded with some exception. Every command AOF0 causes the writing strobe generation, loads instruction register with a code, which produces logic 0 at the ALU output. The writing strobe latches the addressed data in the output register and then its content is transferred through the output logical scheme to the computer memory. DIS can output 16 bit word format. Logical 0 from ALU output applied to the memory data input is used to clear the currently addressed memory cell. In conclusion the writing strobe increments the address counter. Since the memory chip has not reset input, readout and buffer store clearing take place simultaneously. In this way the buffer store is prepared for the next cycle of integration.

Now consider DSI operation in the detection mode. In this mode both fronts of the modulation signal F are used for address counter reseting and instruction code formation in the operation register. Switching to logic 1 causes "reset(det)" signal generation for address counter, sets instruction code corresponding to "A+B" ALU function. Afterwards ALU sums incoming digitized samples of the spectral channels in "Antenna" phase with the contents of currently addressed memory cells. This process is just the same as in the integration mode. Signal modulation F switching to logical 0 initiates the address counter again, but forms a code in the instruction register corresponding to "A-B" ALU function. And now ALU subtracts all the incoming digitized signals of the spectral channels corresponding to "Equivalent" phase from the current memory contents of the same name channels. Timing of this procedure differs from the previous one only by "A-B" ALU function instead of "A+B".

As in the integration mode the final result of detection for N periods of modulation signal may be expressed as follows:

$$D = \left\{ \sum_{i=0}^{N-1} (a_{ki} - e_{ki}) \;\middle|\; k=1,2,\ldots,K \right\},$$

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where a_{ki}, e_{ki} are digitized signals of k-th spectral channel in i-th modulation period. In this mode file D occupies only K memory cells, twice less than in the integration mode. Because of this it takes twice less time for output information. This feature may be useful in the experiments with a high time resolution or with an increased modulation frequency. And, on the other hand, accumulation of difference $(a_{ki} - e_{ki})$ instead of separate integration of a_{ki} and e_{ki} permits to increase greatly the integration time that, in its turn, gives an opportunity to process the output data and to display graphic information in a real time.

There is an opportunity of software testing and diagnostic of all the main units in the DSI. It is possible to load arbitrary codes into the buffer store through the CAMAC bus, execute all the ALU functions. After reading and checking of the results one may appreciate capacity for application. If something is wrong in DSI operation, the failure may be localized very exactly.

The described transference of routine functions, such as integration and detection, from a computer to DSI has allowed to increase the number of frequency channels processed in a real time from 100 (Abramyan et al., 1983) up to 1000. An application of DSI with a filter analyzer instead of analog output units (Grachev and Prozorov, 1976) greatly reduces the system's dimensions, power consumption, excludes precise adjustment and increases reliability and stability.

DSI was used in different experiments (Esepkina et al., 1990; 1992) and proved itself as a suitable and reliable device.

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